automatically generating an output clock signal based on the determining;

wherein receiving the input clock signal comprises receiving a single-ended clock signal on a first input terminal and a ground potential on a second input terminal.

6. (Amended) A method comprising:

receiving a first channel of an input clock signal;

receiving a second channel of the input clock signal, wherein the second channel of the input clock signal is one of a constant signal at ground potential, a constant signal above ground potential or a signal at the same frequency as the first channel of the input clock signal;

automatically generating a single-ended clock signal from the first and second channels of the input clock signal when the second channel of the input clock signal is one of a constant signal above ground potential or a signal at the same frequency as the first channel of the input clock signal; and

automatically generating a single-ended clock signal from the first channel of the input clock signal when the second channel of the input clock signal is a constant signal at ground potential.

9. (Amended) A device comprising:

a first terminal to receive a first channel of a clock input signal;

a second terminal to receive a second channel of the clock input signal; and

a detector coupled to the second terminal to receive the second channel of the clock input signal, wherein the detector is configured to output a clock mode signal as a function of a voltage potential of the second channel of the clock signal.

10. (Amended) A device comprising:

a first terminal to receive a first clock input signal;

a second terminal to receive a second clock input signal;

a detector coupled to the second terminal to receive the second clock input signal, wherein the detector is configured to output a clock mode signal as a function of a voltage potential of the second clock signal;

a first circuit coupled to the first terminal configured to generate a first single-ended clock signal of the same frequency as the first clock input signal;

a second circuit coupled to the first terminal and to the second terminal to generate a second single-ended clock signal of the same frequency as the first clock input signal; and

a selector configured to select the first single-ended clock signal or the second single-ended clock signal based upon the clock mode signal.